**Course Outline** Spring 2017

CSE 231Digital Logic Design **Section:** 4,5

**Course Schedule/Timing:** Lecture – 3 Hours/week, Lab – 3 Hours/week

**Instructor:**Tanzilur Rahman (Tnr)

**Office:**SAC 1022

**Office Hours:**1.00 - 2.15 PM (S,T,M,W)

**Email:**[tanzilur.rahman@northsouth.edu](mailto:tanzilur.rahman@northsouth.edu)

**Phone:**02 55668200 Ext. 6182

**Course Web** : https://sites.google.com/site/neuro11school/

**Lecture Time:** ST 9:40 – 11:10 (Section 4)

ST 11:20 – 12:50 (Section 5)

**Lecture Room:** NAC 922

**Lab Room:** Digital Microprocessor Laboratory, 5th Floor of SAC Building

**Course Objective:**

After the completion of the course, the students will be able to:

1. Apply the principles of Boolean algebra to logic functions.
2. Use K-maps to realize two-level minimal/optimal combinational circuits
3. Understand the operation of latches, flip-flops, counters and registers.
4. Analyze and design sequential circuits built with various flip-flops.
5. Appreciate the ease and versatility of design using programmable logic.

**Course Description:**

This course provides an introduction to logic design and basic tools for the design of digital logic systems.A basic idea of number systems will be provided, followed by a discussion on combinational logic: logic gates, Boolean algebra, minimization techniques, arithmetic circuits (adders, subtractors), basic digital circuits (decoders, encoders, multiplexers, shift registers), programmable logic devices (PROM, PAL, PLA).The course will then cover sequential circuits: flip-flops, state transition tables and diagrams, state minimization, state machines, design of synchronous/asynchronous counters, RAM/ROM design.An introduction to programmable logic will also be provided.

***Pre-requisites*** CSE 225, CSE 173***Corequisites*** CSE 231L

**Textbook:**

Digital Design

By Morris Mano and Michae D. Ciletti, 5th Edition

Digital Design: Principles and Practices, J F Wakerly, 4thed, Prentice Hall, 2005

Digital Logic Techniques, T J Stonham, 3rded, Chapman & Hall, 1996

Or any good textbook on Digital Logic Design

**Distribution of Points:**

\*Digital Laboratory ------------------------------------- 20 %

Attendance ---------------------------------------- 5 %

Projects/Assignments ---------------------------------------- 15 %

Quizzes -------------------------------------------------- 10 %

Term Examination ---------------------------------------- 25 %

Final Examination (comprehensive) ----------------------- 25 %

\*Must obtain 60% marks in CSE231L

**Important Dates:**

Quizzes After completion of every topic

Term Examination TBA

Final Examination (comprehensive) TBA

**Make-up Policy:**

No make-up testes for the missed Term Examinations and Quizzes.

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| ***Course Topics*** | **Min. Coverage** |
| Numerical representation of numbers  Binary, octal, decimal, hexadecimal, complements, signed/unsigned numbers, binary codes, error detecting/correcting codes | 4.5 hours |
| Boolean algebra  Logic gates, Boolean algebra, Boolean functions, canonical and standard forms | 3 hours |
| Combinational logic design  Minimization techniques (Boolean algebra, Karnaugh map), don’t care conditions, universal gate implementation | 4.5 hours |
| Combinational circuits  Analysis, design procedure, binary adder/subtractor, decoders, encoders, multiplexers, combinational logic implementation using decoders and multiplexers | 6 hours |
| Synchronous sequential logic  Sequential circuits, flip-flops, timing diagrams, state transition tables, state transition diagrams (Mealy and Moore models), state minimization and assignment, design implementation | 6 hours |
| Sequential circuits: Registers and counters  Synchronous/Asynchronous counters, registers, shift registers | 3 hours |
| Memory design (RAM, ROM)  Programmable logic:  Implementation of logic functions using programmable logic devices ROM, PLA, PAL | 6 hours |

**Class Structure:**

**1. Lectures :**Attendance and participation of all of them is strongly encouraged.

**2. Laboratory :** You must pass in your lab to attain a passable grade in theory. 20% marks from your lab will be directly added to your theory

**3. Assignments :**You will be given some design assignments. You will use pen and papers and tools to solve those problems.

**4. Projects :**You will have to submit a hardware design project at the end of the semester. You will work on the project as a group.

**5. Exams:** There will be one midterm, one final exam and no make-ups.